REMARKS/ARGUMENTS

In the Office Action mailed August 17, 2009, claims 1-24 were rejected. In response, Applicants hereby request reconsideration of the application in view of the proposed amendments and the below-provided remarks. No claims are added.

For reference, proposed amendments are presented for claims 1, 3, 4, 9, and 17. In particular, the proposed amendment for claim 1 is presented to recite providing the external clock signal to different internal memory blocks according to a predetermined test pattern. The proposed amendments for claims 9 and 17 are presented to recite similar limitations. These proposed amendments are supported, for example, by the subject matter described in the specification at page 6, lines 22-24, as well as the original language of claim 2. Consequently, claim 2 is canceled. The proposed amendments for claims 3 and 4 merely clarify the original language of the claims. These proposed amendments are supported, for example, by the subject matter described in the specification at page 6, lines 25-28, as well as the original language of claims 3 and 4.

Claim Rejections under 35 U.S.C. 112, first paragraph

Claims 1, 9, and 17 were rejected under 35 U.S.C. 112, first paragraph, as purportedly failing to comply with the written description requirement. Specifically, the Office Action states that the specification does not disclose the internal clock signal independent of the duty cycle of the external clock signal. Office Action, 8/17/20, page 3. Additionally, the Office Action states that the specification is silent as to any modification of the duty cycle of the internal clock signal which would allow the duty cycle to differ from that of the external clock signal, and the specification does not disclose a modification of the duty cycle of the internal clock signal, which is dependent on the external clock signal. Id.

Applicants respectfully submit that the indicated limitation is supported by the specification, even though there may not be explicit antecedent basis for the language. The specification at page 4, lines 29-31, provides written description support for the indicated claim language. Specifically, this portion of the specification should be

understood, within the proper context, to mean "the detection of the slow-to-rise and slow-to-fall delay faults depends on the duty cycle of the internal clock signal PHIX and not **[the duty cycle of]** the external clock signal CL." This implicit reference to the duty cycle of the external clock signal is grammatically correct and consistent with the context of the description. Moreover, attempting to construe this portion of the specification without reference to the duty cycle of the external clock signal would render meaningless the explicit reference to the duty cycle of the internal clock signal. Here, although the language of the claims differs somewhat from the actual nomenclature provided in the specification, Applicants respectfully submit that the claim language is nevertheless supported by the specification because the claims recite limitations that are well within the scope of the embodiments explicitly and implicitly described in the specification.

Therefore, Applicants assert the claims are supported by the specification as filed because the language is within the scope of the written description provided in the specification, and the language does not cause confusion as to the meaning of the claims. Accordingly, Applicants respectfully request that the rejections of claims 1, 9, and 17 under 35 U.S.C. 112, first paragraph, be withdrawn.

Claim Rejections under 35 U.S.C. 112, second paragraph

Claims 2-4 were rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In light of the proposed amendments presented herein, Applicants respectfully request that these rejections be withdrawn. Specifically, claim 2 is canceled, and the proposed amendment for claim 1 (which includes similar language) uses different language. In regard to claims 3 and 4, the proposed amendments clarify the relationship between the 50% duty cycle and the internal memory blocks. Accordingly, Applicants respectfully request that the rejections of claims 2-4 under 35 U.S.C. 112, second paragraph, be withdrawn.

Claim Rejections under 35 U.S.C. 103

Claims 1-13, 16-20, 23, and 24 were rejected under 35 U.S.C. 103(a) as being unpatentable over Churchill et al. (U.S. Pat. No. 6,115,836, hereinafter Churchill) in view of Irrinki et al. (U.S. Pat. No. 5,822,228, hereinafter Irrinki) and Savir (U.S. Pat. No. 5,642,362, hereinafter Savir). Additionally, claims 14, 15, 21, and 22 were rejected under 35 U.S.C. 103(a) as being unpatentable over Churchill and Irrinki in view of Choi (U.S. Pat. No. 6,324,115, hereinafter Choi). However, Applicants respectfully submit that these claims are patentable over Churchill, Irrinki, Savir, and Choi for the reasons provided below.

Independent Claim 1

Claim 1 is patentable over the combination of Churchill, Irrinki, and Savir because the combination of cited references does not teach all of the limitations of the claim. Claim 1 recites:

> A method for providing an external clock signal to an internal memory block of a self-timed memory, the method comprising:
>
> receiving an internal clock signal from a clock monitor of the self-timed memory;
>
> receiving an external clock signal, wherein the external clock signal comprises a duty cycle that is different from a duty cycle of the internal clock signal;
>
> receiving a control signal;
>
> providing, in dependence upon the control signal, the internal clock signal to the internal memory block during a normal mode of operation of the self-timed memory, and the external clock signal to the internal memory block during a test mode of the self-timed memory, wherein providing the external clock signal comprises providing the external clock signal to different internal memory blocks according to a predetermined test pattern; and
>
> detecting a slow-to-rise delay or a slow-to-fall delay in response to providing the external clock signal to the internal memory block during the test-mode of the self-timed memory.

(Emphasis added.)

In contrast, the combination of Churchill, Irrinki, and Savir does not teach all of the limitations of the claim. For reference, the Office Action relies on Churchill as purportedly teaching the limitations which relate to providing the external clock signal to

different internal memory blocks according to a predetermined test pattern. Specifically, the Office Action relies on the teachings in Churchill at column 18, lines 46-48 and column 19, lines 5-10. For convenience, these cited portions of Churchill are reproduced below.

> Coupling scan bit b5 to line 912 may be particularly advantageous when the amount of programmable delay provided by programmable delay circuit 902 is insufficient to allow the signal on line 222 to achieve relatively long pulse durations (e.g., hundreds of nanoseconds or microseconds).
>
> Churchill, col. 18, lines 46-51.

> Thus, the function of the burn-in test may be enhanced when bit 5 is enabled, thereby allowing an external clock signal to replace an internal clock signal when the external clock signal has a larger pulse width than that generated internally by clock pulse generator 900.
>
> Churchill, col. 19, lines 5-10.

A review of these specific teachings of Churchill reveals that these teachings do not relate to or teach providing an external clock signal to different internal memory blocks according to a predetermined test pattern. Although the description referenced in column 19 refers to an external clock signal, the indicated description nevertheless is insufficient to teach any conditions related to a predetermined test pattern used to provide the external clock signal to different internal memory blocks. More specifically, although the general description which includes the cited portions of Churchill relates to using an external clock signal which has a larger pulse width than that generated internally by a clock pulse generator, this description is insufficient to teach providing an external clock signal to different internal memory blocks according to a predetermined pattern. Therefore, Churchill does not teach providing an external clock signal to different internal memory blocks according to a predetermined pattern, as recited in the claim.

For the reasons presented above, the combination of Churchill, Irrinki, and Savir does not teach all of the limitations of the claim at least because Churchill does not teach providing an external clock signal to different internal memory blocks according to a predetermined pattern, as recited in the claim. Accordingly, Applicants respectfully

assert claim 1 is patentable over the combination of Churchill, Irrinki, and Savir because the combination of cited references does not teach all of the limitations of the claim.

Independent Claims 9 and 17

Applicants respectfully assert independent claims 9 and 17 are patentable over the proposed combination of cited references at least for similar reasons to those stated above in regard to the rejection of independent claim 1. Each of these claims recites subject matter which is similar to the subject matter of claim 1 discussed above. Although the language of these claims differs from the language of claim 1, and the scope of these claims should be interpreted independently of other claims, Applicants respectfully assert that the remarks provided above in regard to the rejection of claim 1 also apply to the rejections of these claims.

Dependent Claims

Claims 2-8, 10-16, and 18-24 depend from and incorporate all of the limitations of the corresponding independent claims 1, 9, and 17. Applicants respectfully assert claims 2-8, 10-16, and 18-24 are allowable based on allowable base claims. Additionally, each of claims 2-8, 10-16, and 18-24 may be allowable for further reasons.

CONCLUSION

Applicants respectfully request reconsideration of the claims in view of the proposed amendments and the remarks made herein. A notice of allowance is earnestly solicited.

At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account **50-4019** pursuant to 37 C.F.R. 1.25. Additionally, please charge any fees to Deposit Account **50-4019** under 37 C.F.R. 1.16, 1.17, 1.19, 1.20 and 1.21.

Respectfully submitted,

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